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Attorney's Docket No. 42P15685

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of:

Scott A. Hareland et al.

Application No.: 10/607,769

Filed: June 27, 2003

For: NONPLANAR SEMICONDUCTOR
DEVICE WITH PARTIALLY OR FULLY
WRAPPED AROUND GATE ELECTRODE
AND METHODS OF FABRICATION

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Examiner: Unassigned

Art Unit: Unassigned

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Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under
one of the following (as indicated by an "X" to the left of
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X 37 C.F.R. §1.97(b).

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_____ A statement pursuant to 37 C.F.R. §1.97(e) or

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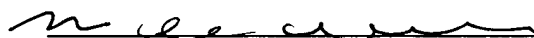
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If there are any additional charges, please charge Deposit Account No. 02-2666.

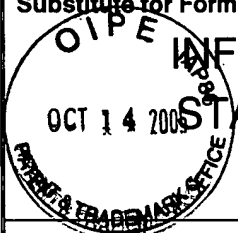
Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 10/12, 2005


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Substitute for Form 1449/PTO  INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Complete if Known		
			Application Number	10/607,769	
			Filing Date	June 27, 2003	
			First Named Inventor:	Scott A. Hareland	
			Art Unit	Unknown	
			Examiner Name	Unknown	
Sheet	1	of	2	Attorney Docket Number	42P15685

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)				
		US-	6,709,982 B1	03/23/2004	Buynoski et al.	
		US-	6,645,797 B1	11/11/2003	Buynoski et al.	
		US-	6,475,869 B1	11/05/2002	Yu	
		US-	5,545,586	08/13/1996	Koh	
		US-	2004/0256647 A1	12/23/2004	Lee et al.	
		US-	2003/0057486 A1	03/27/2003	Gambino et al.	
		US-	2002/0036290 A1	03/28/2002	Inaba et al.	
		US-	2002/0011612 A1	01/31/2002	Hieda	
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FOREIGN PATENT DOCUMENTS						
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		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				
		EP 1 202 335 A	05/02/2002	IBM	Page 6, par 22	
		JP 2002298051	10/17/2003	Lee Soko	Abstract, Fig 11	

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			Art Unit	Unknown	
			Examiner Name	Unknown	
Sheet	2	of	2	Attorney Docket Number	42P15685

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
		BURENKOV, A. et al., "Corner Effect in Double and Triple Gate FINFETs", European Solid-State Device Research, 2003 33 rd Conference on Essderc '03 September 2003, Piscataway, NJ, USA, IEEE, pages 135-138, XP010676716	
		CHANG, S.T. et al, "3-D Simulation of Strained Si/SiGe Heterojunction FinFETS", Semiconductor Device Research Symposium, 2003 International, December 2003, Piscataway, NJ, USA, IEEE, pages 176-177, XP010687197	
		International Search Report PCT/US2005/010505	

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